AP 10578

Claims

1-20. Canceled

21. (New) An analysis device for an embedded system comprising:

a CPU;

a CPU bus;

a memory (3); and

at least one communication module for input or output of analysis data by way of a test interface, wherein the communication module permits the memory and input and output access operations of the embedded system to be monitored and/or logged without using clock cycles of the CPU.

22. (New) The analysis device of claim 21, wherein at least three freely selectable analysis modes, with the analysis modes, in the way and extent of participation of the CPU , differing from each other in the read and/or write operations of data for analyzing purposes.

23. (New) The analysis device of claim 22, wherein depending on the selected analysis mode, either

- all write access operations of the CPU are logged to especially definable address ranges without using clock cycles, or
- all read access operations of the CPU are logged, or
- direct reading and writing of the CPU out of/into an external memory is executed by using clock cycles.

24. (New) The analysis device of claim 23, wherein the communication module comprises a controller which, by way of a connection to at least a data bus, a control bus, or an address bus, can independently make access to the bus of the

embedded system in order to monitor write and/or read access operations in real time, without influencing of the CPU.

25. (New) The analysis device of claim 24, wherein the communication module is connected to a buffer store and the data transferred in write and/or read access operations can be stored in the buffer store.

26. (New) The analysis device of claim 25, wherein the data can be output from the buffer store in a buffered fashion by way of the test interface or data can be read into the buffer store by way of the test interface.

27. (New) The analysis device of claim 23, wherein the external memory is a magnetic core memory or a dual-port memory.

28. (New) The analysis device of claim 21, wherein the communication module is integrated into the embedded system.

29. (New) The analysis device of claim 21, wherein the test interface is connected to a test code memory arranged outside the embedded system.

30. (New) The analysis device of claim 21, wherein the data transfer from the communication module to an external memory takes place by way of a parallel interface.

31. (New) The analysis device of claim 30, wherein the external memory is connected to a data conditioning device providing an interface connection to external debugging applications.

32. (New) An embedded system comprising and analysis device, the embedded system comprising:

a central processor unit;

a CPU bus;

a memory; and

at least one communication module for input or output of analysis data by way of a test interface, wherein the communication module permits the memory and input and output access operations of the embedded system to be monitored and/or logged without using clock cycles of the CPU.

33. (New) A method for analyzing an embedded system comprising:

providing a central processor unit;

providing a CPU bus;

providing a memory;

providing at least one communication module having at least input element and at least one output element;

providing at least one mode for analyzing data in real time without requiring the system to be stopped or interrupted, respectively, for the analysis.

34. (New) The method of claim 33, wherein

- the memory content or a correspondingly assessable information of the embedded system, in whole or in part, is copied in real time into an external memory, with the data being buffered in particular before this operation, and/or
- the data content of an external memory or a correspondingly assessable information about the memory content of the memory, in whole or in part, is copied in real time into a memory of the embedded system, with the data being buffered in particular before this operation.

35. (New) The method of claim 34, wherein the external memory is used to transmit data for typical debugging applications.

36. (New) The method of claim 35, wherein only the data needed for debugging is transferred to the external memory in the event of access operations of the CPU to

RAM.

37. (New) The method of claim 34, wherein at least the write access operations or the read access operations of the CPU are logged by means of a buffer store.

38. (New) The method of claim 37, wherein information about the write access operations is written without additional CPU commands into the buffer store or directly into the communication module, and the information about the read access operations is written into the buffer store with active assistance of the CPU.

39. (New) The method of claim 33, wherein a mode of the embedded system is provided in which all write and/or read access operations of the CPU are rerouted to the communication module.

40. (New) The method of claim 33, wherein a mode of the embedded system is provided in which only either the write access operations or the read access operations of the CPU are rerouted to the communication module, and the other access operations of the CPU to the memory are logged actively by the CPU into the external memory.